BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/914,429	11/05/2001	Masayuki Satoh	HITA.0099	5387

7590 05/02/2003

Stanley P Fisher
Reed Smith Hazel & Thomas
Suite 1400
3110 Fairview Park Drive
Falls Church, VA 22042-4503

EXAMINER
THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/914,429	SATOH ET AL.
	Examiner	Art Unit
	A. M. Thompson	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 11-20* is/are rejected.

7)☒ Claim(s) *8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This application, 09/914,429, with Preliminary Amendment of 05 November 2001, has been examined. Claims 3 and 4 are amended. Claims 17-20 are added. Claims 1-20 are pending.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The claims are directed to a self-construction circuit.

Claim Objections

2. **Claim 8** is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). **Accordingly, the claim has not been further treated on the merits**.

3. **Claims 1, 5, 8-11, 15, 16** are objected to because of the following informalities: Pursuant to **claim 1**, at line 3, change "compare" to - -compares- -; at line 9, before data, insert - -write- -. Pursuant to **claim 5**, change "has the" to - -is a- -. Pursuant to **claim 8**, at line 6, "the self-construction circuit" requires prior antecedent basis or a structural/functional relationship between the claim 8 limitations and the claims from which it depends. Pursuant to **claims 9 and 10**, "the same semiconductor chip" requires prior reference for proper antecedent basis. Pursuant to **claims 15 and 16**, change "semiconductor chip" to - -semiconductor integrated circuit- -. Pursuant to **claim 15**, at line 2, before "converting", insert - -the- -. Pursuant to **claim 11**, at line 2,

change "hold" to - -holds- -; at line 3, before "hardware", insert - -a- -; at line 4, change "obtain' to - -obtains- -; at line 5, "the output terminal" requires prior reference for correct antecedent basis; at line 6, before "address", change "the" to - -an- -. Additionally, pursuant to claim 11, rephrasing of this claim is required so that it is clear what entity obtains the output of the logical function. Claims dependent from the above claims are likewise objected to. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 11-16** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Specifically and pursuant to claim 11, the structural/functional cooperative relationships between the output terminal, the address terminal and the semiconductor integrated circuit and the logical function is unclear. Pursuant to claim 15, the relationship between "converting means" and the rest of the claim is unclear. Further, it is unclear what description, at line 4, is being referenced. Pursuant to claim 16, it is unclear what "the description represented in the hardware description language references.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Rejection of claims 1-7 and 11-20

7. Claims 1-7, 11-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Satou *(sic)* et al., U.S. Patent 6,233,182 (with PCT Pub. Date October 22, 1998) .

8. Pursuant to claim 1, which recites [a] semiconductor integrated circuit comprising storing means (col. 5, ll. 11-14) that enables reading and writing; comparing means (fig. 1, #6; also col. 8, ll. 16-40) that compare write data supplied to the storing means with data read from the storing means; and variable address converting means that converts and address signal to the storing means based on a comparison result in the comparing means, wherein an input signal of a logic circuit (the test circuit, col. 7, line 65 to col. 8, line 8) having a desired logical function is input as the address signal to the storing means and wherein the data is written to the storing means so that the read data of the storing means can be obtained as an expected output signal (the expected value data, col. 8, ll. 16-40) with respect to the input signal of the logic circuit.

9. Pursuant to claim 2, wherein a plurality of the storing means, a plurality of the comparing means, and a plurality of the variable address converting means are provided on a single semiconductor circuit (Fig. 1; col. 7, ll. 33-35).

10. Pursuant to claim 3, wherein the storing means are a volatile memory (Fig. 1, #11; col. 9, ll. 5-9).

11. Pursuant to claim 4, wherein the variable address converting means comprise a memory array in which a plurality of memory cells are arranged in a matrix shape (col.

7, ll. 33-64, which discloses a memory array and an array and matrix are synonymous terms); an address decoder that selects the memory cells in the memory array based on an input address signal (col. 7, ll. 33-64 discloses X and Y decoders); reading means that amplify a signal read from the memory array (col. 7, ll. 33-64 discloses a sense amplifier); and operating means that update the input address signal based on a control signal (col. 7, ll. 33-64 which discloses an internal control circuit).

12. Pursuant to claim 5, wherein the memory array has a volatile memory (claim 34 discloses the instruction memory as a RAM or a dynamic RAM which are volatile memory (col. 9, ll. 5-9).

13. Pursuant to claim 6, further comprising data holding means (col. 9, ll. 5-18) that can hold the data read from the storing means; a switch matrix that switches the input address signal or an output signal of the data holding means and can supply it to the variable address converting means (col. 9, ll. 49-57; Fig. 6, #160); and the storing means that store the control information of each switch in the switch matrix (col. 10, ll. 21-34).

14. Pursuant to claim 7, wherein the data holding means comprise latching means (col. 9, ll. 49-65, the switching circuit) that can latch first data read from the memory circuit (col. 10, ll. 6-20); and gate means that permit or do not permit latching of the first data to the latching means based on the first data read from the memory circuit (col. 21, ll. 45-52)

15. Pursuant to claim 11, comprising storing means that holds information obtained from a description in which a logical function is represented in hardware description

language (col. 3, line 44 to col. 4, line 9; see also col. 22, ll. 38-49) and obtains the output of the logical function that complies with an input signal from the output terminal, using the signal supplied to the address terminal as the input signal (see Fig. 3).

16. Pursuant to claim 12, wherein the logical function includes a combinational logical function (Figs. 5 and 6; see also col. 23, ll. 45-55).

17. Pursuant to claim 13, wherein the logical function includes a sequential logical function (Fig. 5, illustrates a sequence controller; Fig. 1, #13 illustrates a sequence control circuit).

18. Pursuant to claim 14, wherein the storing means are read and write enable storing means (col. 7, ll. 33-64 and especially ll. 51-61).

19. Pursuant to claim 15, wherein converting means that form the information written to the storing means from the description represented in the hardware description language and the storing means are formed on the same semiconductor chip.

20. Pursuant to claim 16, wherein the storing means that hold the description represented in the hardware description language are formed on the semiconductor chip (Fig. 1, #10).

21. Pursuant to claim 17, wherein the storing means are a volatile memory (Fig. 1, #11; col. 9, ll. 5-9).

22. Pursuant to claim 18 (which depends from claim 2), wherein the variable converting means comprise a memory array in which a plurality of memory cells are arranged in a matrix shape (col. 7, ll. 33-64, which discloses a memory array and an array and matrix are synonymous terms); an address decoder that selects the memory

cells in the memory array based on an input address signal (col. 7, ll. 33-64 discloses X and Y decoders); reading means that amplify a signal read from the memory array (col. 7, ll. 33-64 discloses a sense amplifier); and operating means that update the input address signal based on a control signal (col. 7, ll. 33-64 which discloses an internal control circuit).

23. Pursuant to claim 19 (which depends from claim 3), wherein the variable converting means comprise a memory array in which a plurality of memory cells are arranged in a matrix shape (col. 7, ll. 33-64, which discloses a memory array and an array and matrix are synonymous terms); an address decoder that selects the memory cells in the memory array based on an input address signal (col. 7, ll. 33-64 discloses X and Y decoders); reading means that amplify a signal read from the memory array (col. 7, ll. 33-64 discloses a sense amplifier); and operating means that update the input address signal based on a control signal (col. 7, ll. 33-64 which discloses an internal control circuit).

24. Pursuant to claim 20 (which depends from claim 17), wherein the variable converting means comprise a memory array in which a plurality of memory cells are arranged in a matrix shape (col. 7, ll. 33-64, which discloses a memory array and an array and matrix are synonymous terms); an address decoder that selects the memory cells in the memory array based on an input address signal (col. 7, ll. 33-64 discloses X and Y decoders); reading means that amplify a signal read from the memory array (col. 7, ll. 33-64 discloses a sense amplifier); and operating means that update the input

address signal based on a control signal (col. 7, ll. 33-64 which discloses an internal control circuit).

Allowable Subject Matter

25. Claims 9 and 10 contain allowable subject matter.

26. The following is a statement of reasons for the indication of allowable subject matter: Pursuant to claims 9 and 10, Satoh '182 does not disclose a self-construction circuit.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure. Please reference the PTO-892 for a complete listing.

28. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

29. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner

30 April 2003